# ASDM20P50KQ

## -20V P-Channel MOSFET

.

## General Features

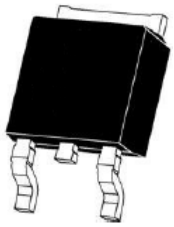
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high $E_{AS}$
- Excellent package for good heat dissipation

## Application

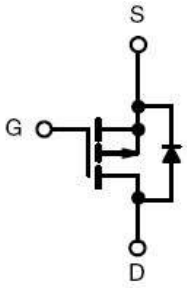
- Load switch
- Battery protection

## Product Summary

| | | |
|---|---|---|
| BVDSS | -20 | V |
| RDS(on)Typ.@VGS=-4.5V | 6.3 | mΩ |
| ID | -50 | A |



TO-252-2L top view




Schematic diagram

## Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | -20 | V |
| Gate-Source Voltage | $V_{GS}$ | ±12 | V |
| Drain Current-Continuous | $I_D$ | -50 | A |
| Drain Current-Continuous($T_C$=100℃) | $I_D$ (100 )℃ | -35 | A |
| Pulsed Drain Current | $I_{DM}$ | -200 | A |
| Maximum Power Dissipation | $P_D$ | 80 | W |
| Derating factor | | 0.64 | W/℃ |
| Operating Junction and Storage Temperature Range | $T_J$,$T_{STG}$ | -55 To 150 | ℃ |

## Thermal Characteristics

| Parameter | Symbol | Limit | Units |
|---|---|---|---|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 1.6 | °C/W |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 50 | °C/W |

## Electrical Characteristics ($T_C$=25℃unless otherwise noted)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V $I_D$=-250μA | -20 | - | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=-16V,$V_{GS}$=0V | - | - | 1 | μA |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$=±12V,$V_{DS}$=0V | - | - | ±100 | nA |
| **On Characteristics** (Note 3) | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$,$I_D$=-250μA | -0.3 | -0.8 | -1.2 | V |
| Drain-Source On-State Resistance | $R_{DS(ON)}$ | $V_{GS}$=-4.5V, $I_D$=-20A | - | 6.3 | 7 | mΩ |
| | | $V_{GS}$=-2.5V, $I_D$=-20A | - | 9.0 | 10 | |
| | | $V_{GS}$=-1.8V, $I_D$=-20A | - | 17 | 22 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$=-5V,$I_D$=-20A | 80 | - | - | S |
| **Dynamic Characteristics** (Note4) | | | | | | |
| Input Capacitance | $C_{lss}$ | $V_{DS}$=-10V,$V_{GS}$=0V, F=1.0MHz | - | 3673 | - | PF |
| Output Capacitance | $C_{oss}$ | | - | 606 | - | PF |
| Reverse Transfer Capacitance | $C_{rss}$ | | - | 467 | - | PF |
| **Switching Characteristics** (Note 4) | | | | | | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$=-10V, $R_{GEN}$=3Ω $V_{GS}$=-4.5V,$R_L$=0.5Ω | - | 18 | - | nS |
| Turn-on Rise Time | $t_r$ | | - | 42 | - | nS |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 85 | - | nS |
| Turn-Off Fall Time | $t_f$ | | - | 23 | - | nS |
| Total Gate Charge | $Q_g$ | $V_{DS}$=-10V,$I_D$=-20A, $V_{GS}$=-4.5V | - | 55 | - | nC |
| Gate-Source Charge | $Q_{gs}$ | | - | 10 | - | nC |
| Gate-Drain Charge | $Q_{gd}$ | | - | 15 | - | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| Diode Forward Voltage (Note 3) | $V_{SD}$ | $V_{GS}$=0V,$I_S$=-20A | - | - | -1.2 | V |
| Diode Forward Current (Note 2) | $I_S$ | | - | - | -50 | A |
| Reverse Recovery Time | $t_{rr}$ | TJ = 25°C, IF = -10A di/dt = 100A/μs (Note3) | - | 47 | - | nS |
| Reverse Recovery Charge | Qrr | | - | 53 | - | nC |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

**Notes:**

**1.** Repetitive Rating: Pulse width limited by maximum junction temperature.
**2.** Surface Mounted on FR4 Board, t ≤ 10 sec.
**3.** Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
**4.** Guaranteed by design, not subject to production

## Typical Electrical and Thermal Characteristics (Curves)

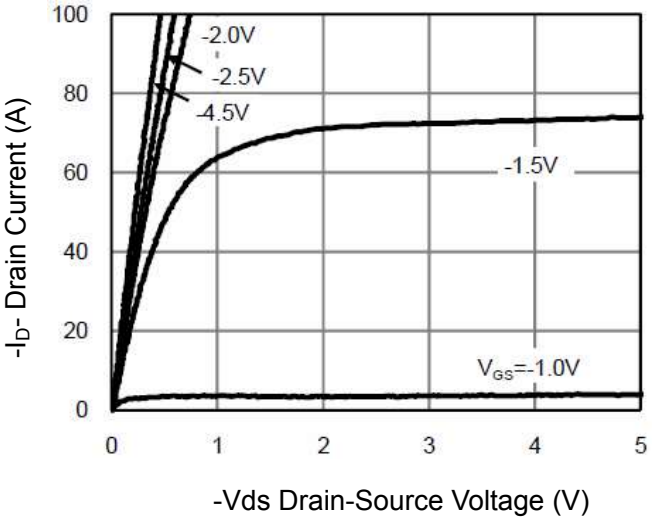



**Figure 1 Output Characteristics**

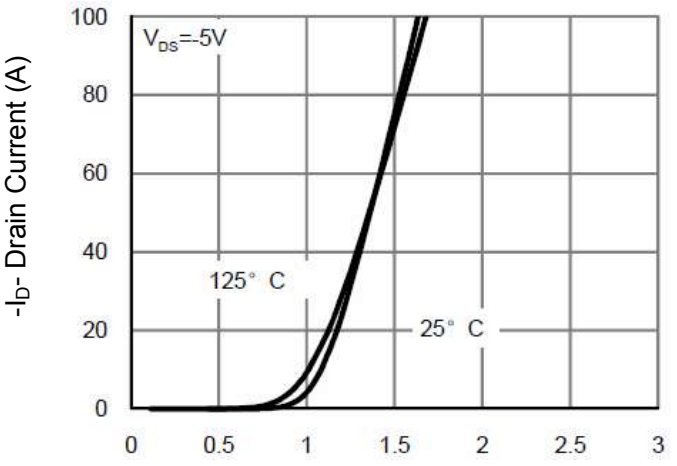



**Figure 2 Transfer Characteristics**

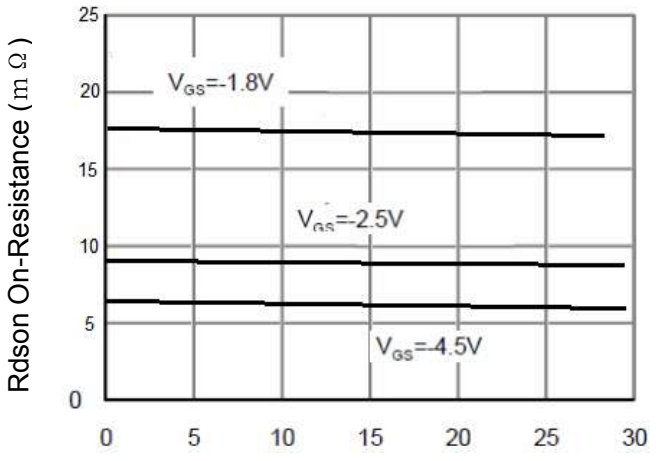



**Figure 3 Rdson- Drain Current**

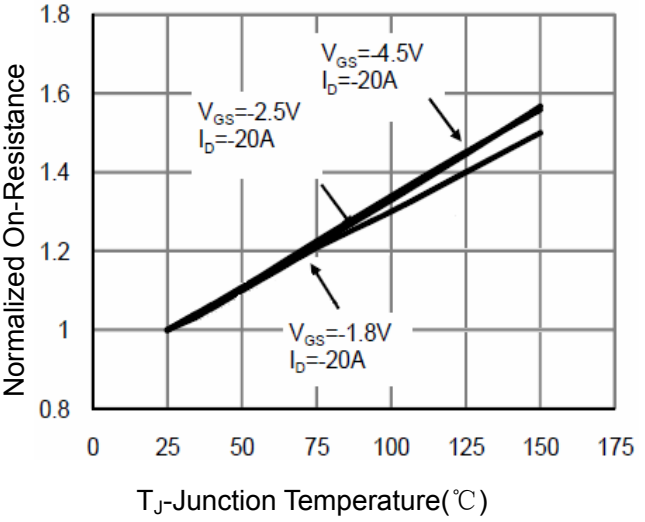



**Figure 4 Rdson-Junction Temperature**

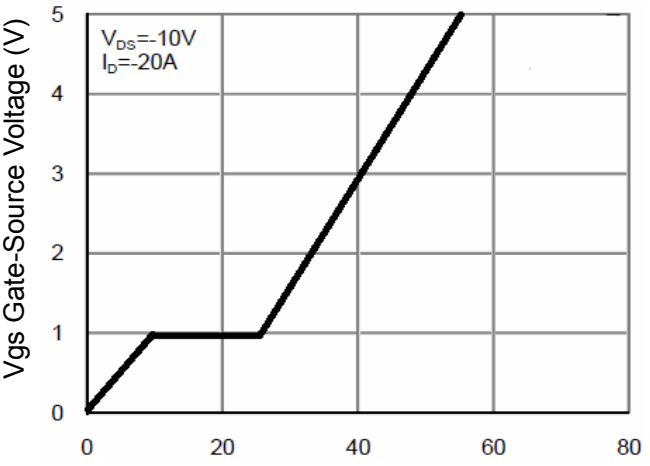



**Figure 5 Gate Charge**

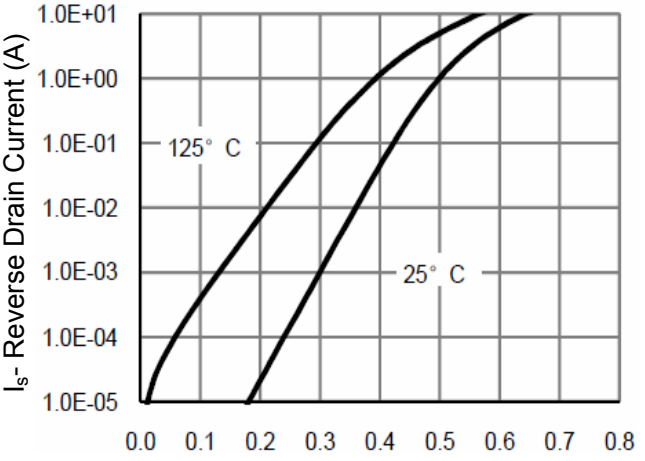
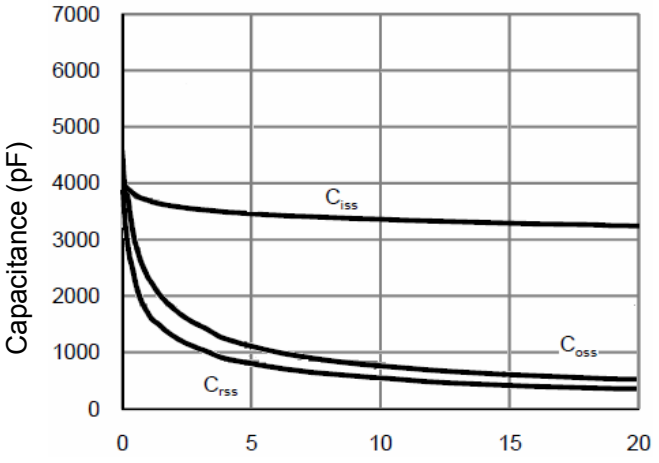
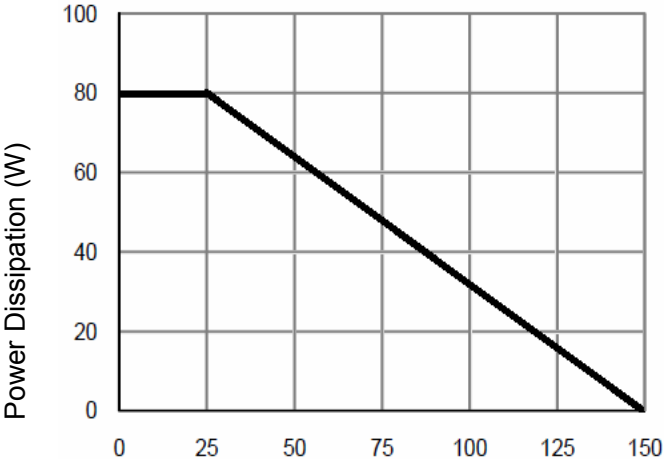



**Figure 6 Source- Drain Diode Forward**



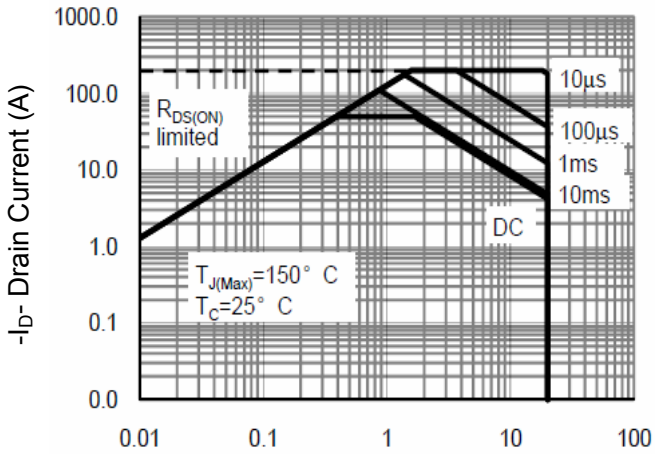

-Vds Drain-Source Voltage (V)

**Figure 7 Capacitance vs Vds**



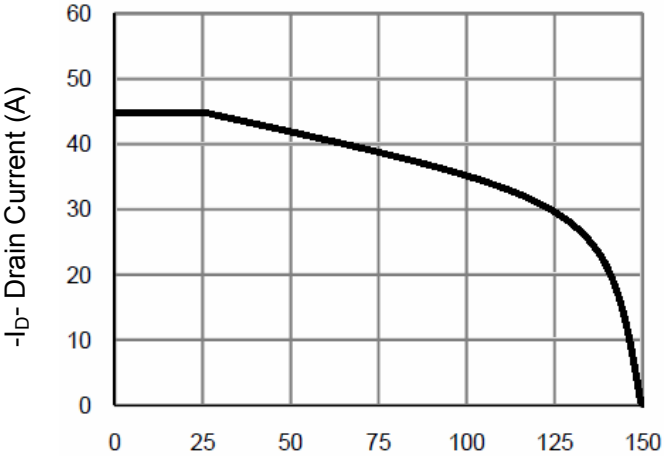

$T_J$-Junction Temperature(℃)

**Figure 9 Power De-rating**



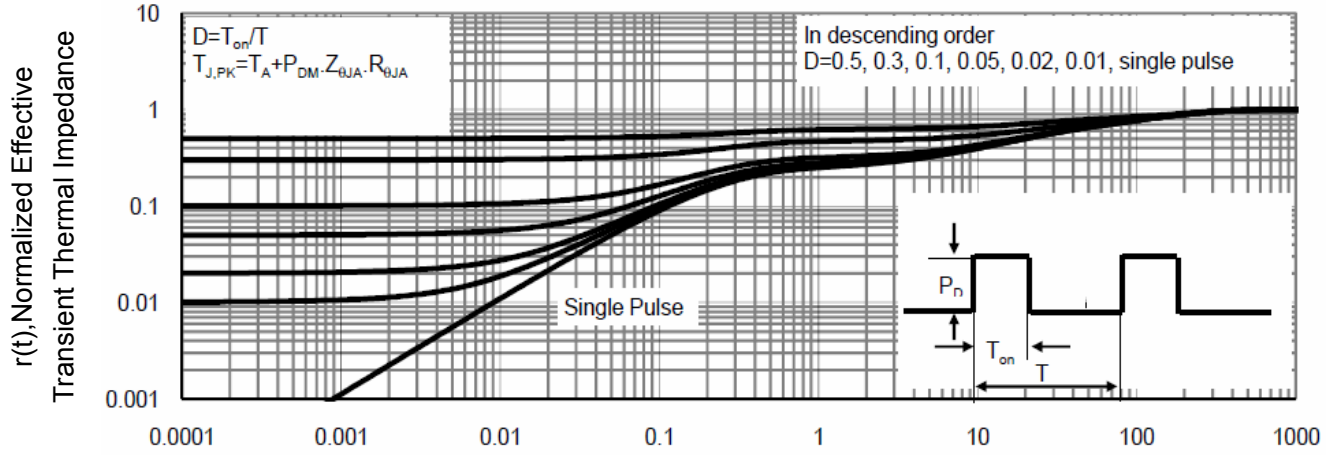

-Vds Drain-Source Voltage (V)

**Figure 8 Safe Operation Area**




$T_J$-Junction Temperature(℃)

**Figure 10 -Current De-rating**

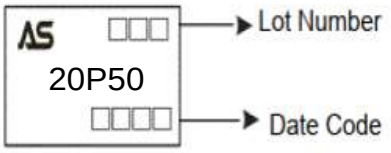



Square Wave Pluse Duration(sec)

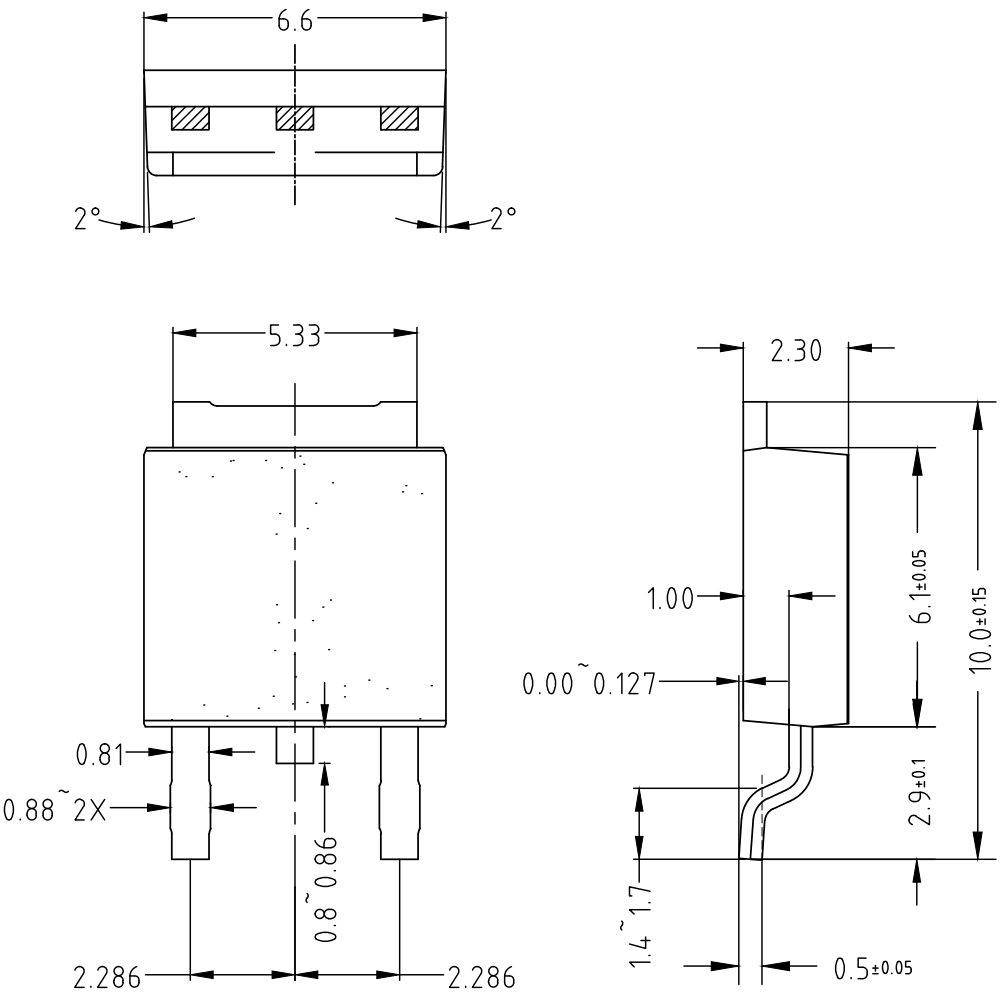
**Figure 11 Normalized Maximum Transient Thermal Impedance**

## Ordering and Marking Information

| Ordering Device No. | Marking | Package | Packing | Quantity |
|---|---|---|---|---|
| ASDM20P50KQ-R | 20P50 | TO-252 | Tape&Reel | 2500/Reel |

| PACKAGE | MARKING |
|---|---|
| TO-252 |  |

# TO-252


6.6
2°
2°
5.33
0.81
0.88~2X
0.8~0.86
2.286
2.286
2.30
1.00
0.00~0.127
6.1±0.05
10.0±0.15
2.9±0.1
1.4~1.7
0.5±0.05

**IMPORTANT NOTICE**

Xi'an Ascend Semiconductor incorporated MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Xi'an Ascend Semiconductor Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Xi'an Ascend Semiconductor Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Xi'an Ascend Semiconductor Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume .

all risks of such use and will agree to hold Ascendsemi Incorporated and all the companies whose products are represented on Xi'an Ascend Semiconductor Incorporated website, harmless against all damages.

Xi'an Ascend Semiconductor Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel. Should Customers purchase or use Xi'an Ascend Semiconductor Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Xi'an Ascend Semiconductor Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

**www.ascendsemi.com**